REMARKS

Entry of this Amendment is proposed because it does not raise any new issues requiring further search, narrows the issues on appeal and does not require further search by the Examiner.

An excess claim fee payment letter is submitted herewith for one (1) excess independent claim.

Claims 1-20 are all the claims presently pending in the application. Claims 2 and 3 have been rewritten merely to place these claims in independent form. Therefore, claims 1-3 and 11 are independent claims.

It is noted that the claim amendments are made only for rewriting claims 2 and 3 in independent form and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Applicant's admitted prior art (hereinafter "APA") in view of Kellogg, et al. (U.S. Patent No. 6,070,262; hereinafter "Kellogg").

This rejections is respectfully traversed in the following discussion.

I. STATEMENT OF SUBSTANCE OF TELEPHONE INTERVIEW/CONFERENCES

Applicant's representative would like to thank the Examiner for courtesies extended in the telephone interview/conferences of June 21, 2004, June 23, 2004, and June 30, 2004.

In the telephone conferences, the Examiner confirmed that newly added claims 15-20 were considered and stand rejected for similar reasons as claims 1-14. Although, as Applicant pointed out, the specific rejection of claims 15-20 were not explained or supported in the text of the rejection.

In the telephonic interview of June 30, 2004, Applicant's representative also discussed the characterization of Figure 3 of the Kellogg reference.

In accordance with the Examiner's request, Applicant has provided a detailed explanation of the mischaracterization of Figure 3 of Kellogg herewith, together with Applicant's further traversal arguments for overcoming the rejections of claims 1-20, for the Examiner's consideration.

II. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor memory device having an error check and correction (ECC) type error recovery circuit.

An illustrative, non-limiting embodiment of the semiconductor memory device, as defined by independent claim 1, includes a memory cell array including at least one

normal memory cell array portion and an ECC memory cell array portion. The normal memory cell array portion includes a plurality of normal memory cells, and the ECC memory cell array portion includes a plurality of ECC memory cells. The device also includes an X decoder for selecting one of word lines in the memory cell array, wherein the word lines extend from the X decoder to the memory cell array, and an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, the cell data including data from normal cells and ECC cells of the selected word line, wherein the ECC memory cell array portion is disposed at a location other than the far end of the word lines from said X decoder.

In another exemplary embodiment, as defined by independent claim 11, the semiconductor memory device having an error check and correction (ECC) type error recovery circuit includes a memory cell array including a plurality of normal memory cell array portions and an ECC memory cell array portion. Each of the normal memory cell array portions includes a plurality of normal memory cells, and the ECC memory cell array portion includes a plurality of ECC memory cells. The device also includes an X decoder for selecting at least one of the word lines in the memory cell array, the word lines in the memory cell array, and the word lines extending from the X decoder to the memory cell array. The device also includes a Y decoder and digit lines extending from the Y decoder toward the memory cell array, and an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line. The cell data includes data from normal cells and ECC cells of the selected word

line, wherein the ECC memory cell array portion is disposed at a location other than the far end of the word lines from the X decoder.

In the present invention, the ECC cell array portion is disposed at a location in which read out speed of data from ECC cell or cells does not become the worst (e.g., slowest) speed in a memory device. That is, the ECC cell array portion is disposed at a location other than at the far end portion of the word lines, with respect to the X decoder.

Thus, the normal cell array portion is disposed at a location in which the read out speed of data from a normal cell becomes the worst speed in a memory device.

Accordingly, the worst read out speed of data can be measured from outside (e.g., the exterior), in order to perform a production test of memory devices, to analyze the cause of a defect in operation speed and the like.

Conventional memory devices that use the ECC type error recovery circuit have several disadvantages. For example, the ECC cells are disposed at far ends of the word lines from an X decoder, and thus, it is impossible to correctly measure, from outside the circuit, the slowest value of the reading out speed of the cell data.

Additionally, in conventional memory cell devices, the ECC cells are disposed at the outermost portions of a memory cell array so that the ECC cells can be omitted from the memory cell array in a memory device which does not need the cells (e.g., a memory cell device having a small memory capacity which would undesirably take up a large amount of area if it included the ECC cells). However, the rising (or falling) time of a word select signal becomes slow at the far end portion of a word line when compared

with that at the near end portion on the side of an X address decoder, and therefore, a read out speed of cell data is slower at the far end portion of a word line.

In the claimed invention, as mentioned above, the ECC cell array portion is disposed at a location other than at the far end portion of the word lines, with respect to the X decoder. As such, Applicant has discovered that the normal cell array portion is disposed at a location in which the read out speed of data from a normal cell or cells becomes the worst speed in a memory device. Accordingly, Applicant has discovered that the worst read out speed of data can be measured from outside, for example, to perform production tests of the memory devices, to analyze the cause of a defect in the operation speed, or the like.

Moreover, Applicant has discovered that, by disposing the ECC cell array portion substantially in the central portion of the memory cell array, the manufacturing yield of the semiconductor memory device can be improved because of an improvement in an error recovery rate. That is, the probability of a defect in a memory cell in the middle or central portion of the memory cell array is lower than the probability of a defect in a memory cell in the peripheral portion of the memory cell array.

III. THE PRIOR ART REJECTION

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Applicant's Admitted Prior Art (APA, particularly Figure 3) in view of Kellogg.

For at least the following reasons, Applicant traverses this rejection.

Applicant's remarks submitted in the Amendment under 37 C.F.R. § 1.111 filed on March 11, 2004 are incorporated herein by reference, for the Examiner's convenience.

A. Mischaracterization of Kellogg

Applicant respectfully submits that the Examiner is mischaracterizing the Kellogg reference, for several reasons.

First, Applicant respectfully submits that Figure 3 of Kellogg is not a layout diagram that shows a layout or location of the memory cell array portions, as alleged.

Instead, Figure 3 of Kellogg shows a circuit diagram and operation thereof (e.g., see also Kellogg at column 3, line 60, to column 4, line 19).

Thus, Applicant respectfully submits that the Examiner is mischaracterizing the Kellogg reference, and therefore, the Examiner's position is moot.

That is, Figure 3 of Kellogg merely depicts a circuit diagram which shows that one of the memory arrays 1-8 is selected by a page decoder 162, and that 64 bits of one segment of a selected array are output by using a logic decoder 166. Also, Figure 3 depicts that, when a mode select block 170 is set for ECC mode, 64 bits of one segment within an ECC array are read out by using an ECC decoder and sent to 1 of 8 data decoders 176.

Thus, Figure 3 of Kellogg clearly is not a layout diagram (i.e., Figure 3 does not disclose or suggest a layout or location of memory cell array portions), as alleged by the

Examiner, but instead, merely is a circuit diagram which does not disclose or suggest the physical layout or location of the memory cell array portions.

On the other hand, the Examiner alleges that, in Figure 3 of Kellogg, an ECC array 164' is arranged at the near end of the decoder and, therefore, that it would have been obvious to a person of ordinary skill in the art to arrange the ECC memory location in different areas (locations) of the memory device as allegedly designated by Kellogg (e.g., see Office Action at page 4, lines 14-20).

However, even assuming *arguendo* that the ECC decoder of Kellogg could be compared to the X decoder of the present invention and that Figure 3 of Kellogg could be compared to a layout diagram, Applicant respectfully submits that arrays 1-8 are all disposed at the near end of the decoders 178 and 166.

That is, all of the arrays 1-8 are disposed equidistantly from the decoders.

Thus, in Kellogg, the concept of "far end" and "near end" itself does not exist, and indeed, is not disclosed or suggested by the Kellogg reference. This would be true even if the ECC array were disposed at any other location.

Therefore, for at least the foregoing reasons, Applicant respectfully submits that Kellogg does not disclose or suggest that an "ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder", as recited, for example, in independent claim 1.

Moreover, even assuming *arguendo* that Kellogg would disclose the layout or location of the memory cell arrays, Kellogg still would not disclose or suggest that an

"ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder", as claimed, since Kellogg discloses that all of the arrays 1-8 are disposed equidistantly from the decoders.

Thus, Applicant respectfully submits that it would not have been obvious to modify the Admitted Prior Art based on Kellogg to arrive at the claimed invention, absent impermissible hindsight based analysis.

B. Claims 1, 4-11, and 14:

Moreover, in the Response to Arguments, the Examiner alleges that "*Kellogg's system further teaches to eliminate the need for extra parity memory chips for high performance memory systems with error checking capability*" (see Kellogg at column 2, lines 8-12) "*which means eliminating extra memory chips would improve the speed of reading memory data. Therefore, the application's arguments, although acknowledged, has not been found to be convincing.*" (see Office Action at page 2, lines 11-18).

Applicant respectfully disagrees with the Examiner's position for several reasons.

Applicant respectfully submits that merely eliminating extra memory chips to improve the speed of reading memory data still does not disclose, suggest, or even contemplate the claimed invention.

For example, independent claim 1 recites, *inter alia*, that an "ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder".

That is, the claimed invention does not merely eliminate extra memory chips to improve speed of reading memory data.

Instead, the claimed invention has identified and discovered that by disposing the ECC memory cell array portion at a location other than the far end of the word lines from the X decoder, the normal cell array portion can be disposed at a location in which the read out speed of data from a normal cell or cells becomes the worst speed in a memory device.

Thus, according to the claimed invention, the worst read out speed of data can be measured from outside, for example, to perform production tests of the memory devices, to analyze the cause of a defect in the operation speed, or the like (e.g., see specification at page 7, lines 10-14).

For the foregoing reasons, Applicant respectfully submits that the alleged aspect of eliminating the need for extra parity memory chips for high performance memory systems with error checking capability in Kellogg does not establish a reasonable motivation for modifying the APA based on Kellogg to arrive at the claimed invention.

Instead, such a motivation reasonably merely would lead a person of skilled in the art to eliminate extra parity chips, not to arrive at an "ECC memory cell array portion is disposed at a location other than the far end of said word lines from said X decoder", as claimed in independent claim 1.

The Examiner also asserts that:

> *Kellogg in Figure 3 (sic) element 164' discloses (sic) an ECC array other than far end and further based on the Applicant's*

> *(sic) argument (any location for the ECC is acceptable), the Examiner would like to point out that if the system of Kellogg accepted any location, that means it can also allow the ECC array to dispose in locations including other than far end or central. Therefore, the applied references have been applied appropriately.*

(see Office Action at page 2, line 19, to page 3, line 4; emphasis added).

Applicant respectfully disagrees with the Examiner's position for several reasons.

As the Examiner well knows, the mere fact that references may be capable of being combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of such a combination (see M.P.E.P. § 2143.01).

The Examiner must present a convincing line of reasoning as to why the ordinary skilled artisan would have found the claimed invention to have been obvious in light of the teachings of the references, without the benefit of Applicant's own invention. In doing so, each reference as a whole must be considered for what it fairly teaches to a person of ordinary skill in the art.

Applicant submits that a person of ordinary skill in the art would not have been motivated to modify the APA based on the teachings of Kellogg to arrive at the claimed invention.

That is, neither the APA nor Kellogg, either alone or in combination, teaches or suggests affirmatively and purposefully disposing the ECC memory cell array portion at a particular location other than the far end of the word lines from the X decoder, as claimed in claim 1.

Indeed, the Examiner specifically acknowledges that "the admitted prior art in view of Kellogg et al. does not teach a *specific* location such as at the middle, or close (approximately) to the central" (see Office Action at page 5, lines 5-6).

For example, with reference to Figure 3, Kellogg specifically states that "in this example, sub-page array 164' is predesignated as the check bit array, although *any* sub-page may be chosen for the ECC array" (see Kellogg at column 4, lines 6-8; emphasis added).

Thus, Kellogg clearly does not teach or suggest, either alone or in combination with the APA, affirmatively and purposefully disposing the ECC memory cell array portion at a particular location other than the far end of the word lines from the X decoder, as claimed in independent claim 1.

That is, contrary to the claimed invention, Kellogg discloses that any location for the ECC array is acceptable. This clearly is contrary to the claimed invention, which specifically discloses that positioning the ECC memory cell at the far end of the word lines from the X decoder is unacceptable.

Furthermore, Kellogg does not disclose, suggest, or for that matter, even mention or recognize, any advantages (or disadvantages) stemming from the location of the sub-page array 164' (at any location).

That is, neither the APA nor Kellogg, either alone or in combination, contemplates the problems that are addressed and solved by the claimed invention, recognizes any advantages or disadvantages derived from disposing the ECC memory cell array portion

at a location other than the far end, or for that matter, identifies the criticality of disposing the ECC memory cell as claimed.

On the other hand, assuming *arguendo* that it would have been obvious to combine the APA and Kellogg, Applicant respectfully submits that the resulting combination still would not arrive at the claimed invention.

As mentioned above, Applicant respectfully submits that the Examiner is mischaracterizing the Kellogg reference. That is, Kellogg does not disclose or suggest a layout or location of the logic decoders, as alleged, but instead, merely discloses a circuit diagram and operation thereof.

Further, with respect to independent claims 1 and 11, Applicant respectfully submits that the logic decoder described in Kellogg clearly is different than the X decoder (word decoder) recited in independent claims 1 and 11.

Moreover, the Examiner has not explained or even mentioned how the X and Y decoders of the APA would be combined with the logic decoder of Kellogg, as recited, for example, in independent claim 11.

Thus, Applicant respectfully submits that any combination of the APA and Kellogg would not arrive at the claimed invention, in as complete detail as recited in the claimed invention.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 11 would not have been obvious over the APA in view of Kellogg.

Accordingly, the § 103 rejection of claims 1, 4-11, and 14 should be withdrawn, and these claims permitted to pass to immediate allowance.

C. Claims 2, 3, 12, and 13:

Claims 2 and 3 are rewritten in independent form herewith.

With respect to claims 2, 3, 12, and 13, the Examiner maintains that claims 2, 3, 12, and 13 would have been obvious from the APA in view of Kellogg.

Applicants submit that claims 2 and 3 are patentable for at least the reasons set forth above with respect to independent claims 1 and 11, from which they depend, as well as for the additional features recited therein.

Moreover, Applicant respectfully submits that the Examiner also has not responded to Applicant's traversal position with respect to claims 2, 3, 12, and 13, and also has not cited a reference in support of the Examiner's assertion that "*configuring the ECC cell array in different memory locations is common practice for most error recovery systems*", and therefore, that "*it would have been obvious to implement the ECC cell array in different memory locations*" "*in order to heighten the decoding efficiency and increase the flexibility of configuration*" (see Office Action at page 5, lines 1-11; emphasis added).

Applicant respectfully reiterates that mere conclusory statements are not sufficient to establish a *prima facie* case of obviousness.

It is noted that official notice, which is unsupported by documentary evidence, should only be taken where the facts asserted to be well-known, or to be common knowledge in the art, are capable of instant and unquestionable demonstration as being well-known (see M.P.E.P. § 2144.03).

Applicant has submitted that configuring the ECC cell array in the novel and unobvious manner claimed by Applicant is not common practice and has requested that the Examiner cite a reference in support of this position.

However, in the present Office Action, the Examiner has maintained this position without responding to Applicant's traversal position and without citing a reference in support of this position.

Therefore, Applicant reiterates the request that the Examiner cite a reference in support of this position, and further, that the Examiner respond to Applicant's traversal positions.

Applicant respectfully submits that it would not have been obvious to combine the APA with Kellogg to arrive at the claimed invention as alleged by the Examiner and that the Office Action has not established a *prima facie* case of obviousness with respect to at least the rejection of these claims.

For example, independent claim 2 recites, *inter alia*, "wherein said ECC memory cell array portion is disposed at a middle portion of said memory cell array" (emphasis added).

On the other hand, independent claim 3 recites, *inter alia*, "wherein said ECC memory cell array portion is disposed substantially at the central portion of said memory cell array" (emphasis added).

Claim 12 recites, *inter alia*, wherein said ECC memory cell array portion is disposed at a middle portion of said memory cell array.

Similarly, claim 13 recites, *inter alia*, "wherein said ECC memory cell array portion is disposed substantially at the central portion of said memory cell array" (emphasis added).

By disposing the ECC cell array portion substantially in the central portion of the memory cell array according to an exemplary embodiment of the invention, the manufacturing yield of the semiconductor memory device can be improved because of an improvement in an error recovery rate (e.g., see specification at page 18, lines 23-27). That is, the probability of a defect in a memory cell in the middle or central portion of the memory cell array is lower than the probability of a defect in a memory cell in the peripheral portion of the memory cell array (e.g., see specification at page 18, line 27, to page 19, line 6).

In the Office Action, the Examiner specifically acknowledges that "the admitted prior art in view of Kellogg et al. does not teach a specific location such as at the middle, or close (approximately) to the central" (see Office Action at page 5, lines 5-6).

Such conclusory statements, however, without supporting documentary evidence clearly are not sufficient to establish a *prima facie* case of obviousness.

Therefore, because the Examiner not cited a reference other evidence in support of his position, Applicant respectfully submits that the rejection of claims 2, 3, 12, and 13 should be withdrawn and claims 2, 3, 12, and 13 permitted to pass to immediate allowance.

D. Claims 15-20:

With respect to previously presented claims 15-20, Applicant respectfully submits that neither the APA nor Kellogg, either alone or in combination, discloses or suggests all of the features of these claims for somewhat similar reasons as those set forth above with respect to claims 2, 3, 12, and 13.

Moreover, the Office Action does not cite support for, or for that matter even mention, how the alleged combination of the APA and Kellogg disclose or suggest the additional features recited in claims 15-20.

As mentioned above, the Examiner confirmed in the telephonic conferences that claims 15-20 stand rejected for similar reasons as previously rejected claims 1-14.

However, Applicant respectfully submits that merely grouping the newly added claims 15-20 into the previously stated grounds of rejection of claims 1-14, without identifying or mentioning how the features of the newly added claims 15-20 are disclosed or suggested by the alleged combination of the APA or Kellogg, is not sufficient to establish a *prima facie* case of obviousness at least with respect to the newly added claims 15-20.

That is, Applicant respectfully submits that claims 15-20 recite separate and distinct features of the novel and unobvious invention which are not recited in claims 1-14.

For example, claim 15 recites, *inter alia*, "wherein sad ECC memory cell array portion is disposed at a location other than the far end and a near end of said word lines from said X decoder" (emphasis added).

Claim 16 recites, *inter alia*, "wherein sad ECC memory cell array portion is disposed at a location on said word lines between locations of at least two of the plurality of normal memory cells on said word lines".

Claim 17 recites, *inter alia*, "wherein a selection time of said ECC memory cells in said ECC memory cell array portion is less than a selection time of at least one of the plurality of normal memory cells in said normal memory cell array.

Claim 18 recites, *inter alia*, "wherein a read out speed of data from said ECC memory cells in said ECC memory cell array portion is less than a read out speed of at least one of the plurality of normal memory cells in said normal memory cell array" (emphasis added).

Claim 19 recites, *inter alia*, "wherein said ECC memory cell array portion is disposed at a location on said word lines for limiting a time for selecting said ECC memory cells in said ECC memory cell array portion to a time that is less than a time for selecting at least one of the plurality of normal memory cells in said normal memory cell array" (emphasis added).

Claim 20 recites, *inter alia*, "wherein said ECC memory cell array portion is disposed at a location on said word lines for limiting a read out speed of data from said ECC memory cells in said ECC memory cell array portion to a read out speed that is less than a read out speed of at least one of the plurality of normal memory cells in said normal memory cell array" (emphasis added).

Moreover, the clear advantages over the prior art of the separate and distinct features of the exemplary embodiments of the novel and unobvious invention, as defined by claims 15-20, clearly are described in the present application (e.g., see specification at page 17, line 26, to page 19, line 6).

Therefore, the grounds of rejection of claims 1-14 set forth in the present Office Action are not applicable to claims 15-20, nor sufficient to establish a *prima facie* case of obviousness of claims 15-20.

For at least the foregoing reasons, Applicant respectfully submits that a *prima facie* case of obviousness has not been established at least with respect to the newly added claims 15-20.

Moreover, for somewhat similar reasons as those set forth above, Applicant respectfully submits that neither the APA nor Kellogg, either alone or in combination, discloses or suggests all of the recitations of claims 15-20.

Accordingly, the Examiner respectfully is requested to withdraw this rejection and permit at least claims 15-20 to pass to allowance.

IV. CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.